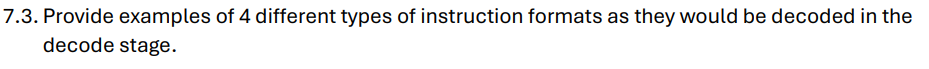
Omar sharafi and Muhamed Biadsy Preparation report :

1)

SweRV EH1 Has 9 pipeline stages.

2)

We can prosses at most 2 commands in the commit step.

3)

R-Type, I-Type, S-type(for load), UJ-type (jumps).

4)

The multiply pipe contains a 3-cycle integer multiplier using three stages (M1, M2, and M3) , this is without the fetch, decode and commit ( with it it will take 9 cycles)

5)

the processor has an out-of-pipeline divider with a 34-cycle latency , so it will take fetch, decode + out of line devide + commit -> 34 + 6 = 40 cycles.

6)

A stall is a deliberate delay introduced into the processor pipeline to resolve a dependency or hazard, it is done by inserting NOPS (no-operation instructions) or using special hardware mechanisms to hold up the pipeline.

So we can say the while NOP is an instructions that does nothing, stall is using that instrction to create a deliberate delay introduced into the processor pipeline to resolve a dependency or hazard.

7)

Four stall points (delays in the processor pipeline caused by dependencies or resource conflicts) exist in the pipeline: ‘Fetch 1’, ‘Align’, ‘Decode’, and ‘Commit’.

8)

A data hazard happens when you must wait for an operand to be computed from some previous step while A control hazard happens when a CPU can't tell which instructions it needs to execute next.

9 + 10)

A screen shot of a computer program

Description automatically generated 